

AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:

assigning a number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and

forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period.

2. (Previously Presented) The method of claim 1 and further comprising for each second address, writing grant information to the memory about the corresponding device.

3. (Previously Presented) The method of claim 2 wherein each device is assigned only consecutive first addresses.

4. (Currently Amended) ~~The method of claim 3 wherein~~ A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:

assigning a number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits, each device being assigned only consecutive first addresses, first addresses are being assigned to a first device, and second addresses are being formed for the first device before first addresses are assigned to a second device;

forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period; and

for each second address, writing grant information to the memory about the corresponding device.

Claims 5-6 (Cancelled)

7. (Currently Amended) ~~The method of claim 1 wherein forming further includes:~~ A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:  
assigning a number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and  
forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period, the sequence of bits being rearranged by:  
    setting a least significant bit of a second address to have a value equal to a most significant bit in a first address; and  
    setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the first address.

8. (Previously Presented) The method of claim 7 and further comprising setting a second next to the least significant bit of the second address to have a value equal to a second next to the most significant bit in the first address.

9. (Cancelled)

SUPPLEMENTAL  
AMENDMENT UNDER 37 CFR §1.116,  
EXPEDITED PROCEDURE REQUESTED

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10. (Currently Amended) ~~The method of claim 1 wherein forming further includes:~~ A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:

assigning a number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and

forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period, the sequence of bits being rearranged by:

gray encoding a first address to form an intermediate address;

setting a least significant bit of a second address to have a value equal to a most significant bit in the intermediate address; and

setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the intermediate address.

11. (Cancelled)

12. (Previously Presented) The method of claim 10 and further comprising setting a second next to the least significant bit of the second address to have a value equal to a second next to the most significant bit in the intermediate address.

Claims 13-16 (Cancelled)

17. (Currently Amended) ~~The communications circuit of claim 16~~  
~~wherein~~ A communications circuit comprising:  
a transmit circuit that transmits information onto a bus;  
a receive circuit that receives information from the bus;  
a memory that stores information on a series of arbitration periods; and  
a logic circuit connected to the transmit circuit, the receive circuit, and the  
memory, if grant information for a group of devices is to be added to the memory, the  
logic circuit assigns a number of first addresses to the group of devices such that two  
or more consecutive first addresses are assigned to each device and no two devices  
have the same first addresses, the number of first addresses representing a  
corresponding number of arbitration periods such that each first address represents  
one arbitration period, each first address having a sequence of bits, the logic circuit  
~~forms~~ forming a number of second addresses from the number of the first addresses  
such that each first address has a corresponding second address and each second  
address has a corresponding device by rearranging the sequence of bits in a plurality  
of the number of first addresses, each second address representing one arbitration  
period.

18. (Currently Amended) ~~The communications circuit of claim 17~~  
~~wherein~~ A communications circuit comprising:

a transmit circuit that transmits information onto a bus;  
a receive circuit that receives information from the bus;  
a memory that stores information on a series of arbitration periods; and  
a logic circuit connected to the transmit circuit, the receive circuit, and the  
memory, if grant information for a group of devices is to be added to the memory, the  
logic circuit assigns a number of first addresses to the group of devices such that two  
or more consecutive first addresses are assigned to each device and no two devices  
have the same first addresses, the number of first addresses representing a  
corresponding number of arbitration periods such that each first address represents  
one arbitration period, each first address having a sequence of bits, the logic circuit  
forming a number of second addresses from the number of the first addresses such  
that each first address has a corresponding second address and each second address  
has a corresponding device by rearranging the sequence of bits in a plurality of the  
number of first addresses, each second address representing one arbitration period,  
the logic circuit forms forming the second addresses by:

setting a least significant bit of a second address to have a value equal  
to the most significant bit in a first address; and

setting a first next to the least significant bit of the second address to  
have a value equal to a first next to the most significant bit in the first address.

19. (Previously Presented) The communications circuit of claim 17 wherein the logic circuit forms the second addresses by:

- gray encoding a first address to form an intermediate address;
- setting a least significant bit of a second address to have a value equal to the most significant bit in the intermediate address; and
- setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the intermediate address.

Claims 20-21 (Cancelled)

22. (Previously Presented) A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:

- assigning a number of first addresses to a device, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits;
- forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses, the first addresses and second addresses having an equal number of bits, each second address representing one arbitration period; and
- storing information in the memory about the device at each location defined by a second address.

23. (Previously Presented) The method of claim 22 wherein the rearranging includes:
- setting a least significant bit of a second address to have a value equal to a most significant bit in a first address; and
  - setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the first address.
24. (Previously Presented) The method of claim 23 wherein the rearranging further includes setting a second next to the least significant bit of the second address to have a value equal to a second next to the most significant bit in the first address.
25. (Previously Presented) The method of claim 22 wherein forming further includes:
- gray encoding a first address to form an intermediate address;
  - setting a least significant bit of a second address to have a value equal to a most significant bit in the intermediate address; and
  - setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the intermediate address.



26. (Previously Presented) A method of adding grant information to a memory that stores information on a series of arbitration periods, the method comprising:

assigning a number of first addresses to a device, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, no two first addresses being identical, each first address having a sequence of bits; and

forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period, no two second addresses being identical.

27. (Currently Amended) ~~The method of claim 26 and further comprising~~ A method of adding grant information to a memory that stores information on a series of arbitration periods, the method comprising:

assigning a number of first addresses to a device, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, no two first addresses being identical, each first address having a sequence of bits;

forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period, no two second addresses being identical; and

storing information in the memory about the device at each location defined by a second address.

28. (Previously Presented) The method of claim 27 wherein the rearranging includes:

- setting a least significant bit of a second address to have a value equal to a most significant bit in a first address; and
- setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the first address.

29. (Previously Presented) The method of claim 28 wherein the rearranging further includes setting a second next to the least significant bit of the second address to have a value equal to a second next to the most significant bit in the first address.

30. (Currently Amended) The method of claim 26 27 wherein forming further includes:

- gray encoding a first address to form an intermediate address;
- setting a least significant bit of a second address to have a value equal to a most significant bit in the intermediate address; and
- setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the intermediate address.